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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,458	KWAK ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-11 and 13-18* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Dec 6, 2004 has been reviewed and considered with the following results:

Some amended changes to the disclosure overcame the objections to the drawings described in the previous Office Action. Therefore, those objections have been withdrawn, and the drawings have been approved by the examiner.

Although the objection to page 1, line 12 has been overcome by the amendment, and now is withdrawn, the objection to page 8, lines 12-13 is basically maintained. A modified objection is described later under the appropriate section, and related comments are described under the Response to Arguments section.

Amended claim 11 overcame its objection, which has been withdrawn. However, after reconsidering the amended claims, a new objection was noted in claim 1. This is described later under the appropriate section.

Amended claim 9 overcame its rejection under 35 U.S.C. 112, and that rejection has now been withdrawn.

Related to the objection on page 8, the rejections of claims 17-18 under 35 U.S.C. 112 are maintained because the source and gate of the PMOS transistor are not connected together as claim 17 implies. A modified rejection is described later under the appropriate section.

The cancellation of claim 2 rendered is rejections moot.

The amended claims, and/or arguments, overcame the rejections of claims 1, 5-9, and 13-15 under 35 U.S.C. 102(b) with respect to Viehmann, and the rejections of claims 1, 3, 5-9, and

13-16 under 35 U.S.C. 103(a) with respect to the applicants' own Prior Art Fig. 2. Viehmann shows only a single MOS transistor, and does not clearly show a reference voltage output node located on the second current path; and the applicants indicate their prior art does not provide sufficient teachings or suggestions to make the obvious type rejections. Therefore, all the original prior art rejections described in the previous Office Action have been withdrawn. However, after reconsidering the Viehmann reference, the claims are now rejected under 35 U.S.C. 103(a) as described later. Also, a reference was found during the update search. The reference of Taguchi teaches/suggests replacing a resistor with a MOS transistor, and shows a circuit directly corresponding to the applicants' own Prior Art Fig. 2, Therefore, some claims are now rejected with respect to the reference of Taguchi.

Although the previous Office Action had indicated claims 4 and 10-11 were only objected to, and they contained allowable subject matter, the allowability of those claims with respect to "a plurality of MOS transistors" limitation has now been withdrawn. After reconsidering the claimed limitations, and performing an update search, the use of a plurality of series connected MOS transistors instead of a single MOS transistor, would be obvious to one of ordinary skill in the art. Therefore, claims 4 and 10-11 are now rejected under 35 U.S.C. 103(a) as described later.

Since these new claim rejections, related to previously indicated allowable material, are made within this action, this action is NON-FINAL.

Specification

The disclosure remains objected to because of the following informality: It is suggested the sentence "The source of...PMOS transistor Q13" on page 8, lines 12-13 be deleted because it

is incorrect. Fig. 3 does not show the (control) gate of Q13 being connected to the source of Q13. An appropriate correction is required.

Claim Objections

Claims 1, 3 and 5 are objected to because of the following informalities: To improve word flow, it is suggested --a-- be added prior to "plurality" on line 2 of claim 1. Dependent claims carry over any objection(s) within any claim(s) upon which they depend. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-18 remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The limitation on lines 4-5 of claim 17 (i.e. "a source of the PMOS transistor...is connected to the gate of the PMOS transistor") is misleading and/or inaccurate because it implies the source of the PMOS transistor is actually connected to its own gate, which does not accurately correspond to the applicants' own figures. For example, using the applicants' own Fig. 5 as a reference, Q31 corresponds to the claimed PMOS transistor, and Q17 corresponds to the first MOS transistor. Although the gate of Q31 is clearly shown coupled to the drain of Q17, the source of Q31 is coupled directly to Evcc, and to the back gate of Q31. The source is not coupled to the (control) gate of Q31.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Oh, a reference found during the recent update search. Fig. 4 shows one type of reference voltage generating circuit comprising an active resistance part (e.g. 330 when 310 is conducting; and 330,340 when 322 is conducting), wherein each of 330 and 340 has a plurality of MOS transistors (i.e. 331-332 for 330; and 341-344 for 340) connected between external voltage VCC and ground voltage VSS. The gate of each transistor receives enable voltage VPP at a potential higher than the drain-source potentials of each of the transistors (e.g. is higher than VCC: see column 6, lines 12-15), and they operate in the linear current-voltage region (e.g. see column 6, lines 16-17). Since the gate electrode of each of transistors 331-332 and 341-344 is connected in common to receive enable voltage VPP, claim 1 is anticipated. When 322 is conducting, transistors 341-344 and 331-332 are all connected in series between external voltage VCC and ground voltage VSS, thus anticipating claim 3. It is understood that some type of circuit, not shown, supplies enable voltage VPP. Deeming that circuit a voltage supply circuit, claim 5 is also anticipated.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-11, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viehmann's PCT WO 01/61430 A1, (published in German on Aug 23, 2001), a reference cited in the previous Office Action. [Note: Viehmann's U.S. Patent 6,586,919 B2 (filed Aug 15, 2002), is considered an acceptable English translation of the PCT reference used in the above rejections.] Fig. 2 shows one type of reference voltage generating circuit comprising active resistance part 22 having single MOS transistor 22, wherein the circuit is connected between external voltage U_{DD} and a ground voltage (not labeled). The gate electrode of MOS transistor 22 receives enable voltage U_E, which is understood to have a higher potential than the drain to source voltage of MOS transistor 22, thus allowing MOS transistor 22 to operate in a linear current-voltage region (e.g. see page 5, lines 5-15 with respect to "Drain-Source-Spannung...60 mV"; "Eingangsspannung zwischen 2 und 5 Volt"; "Gate-Source-Spannung... Eingangsspannung"; "als "linearer Bereich" oder "aktiver Bereich"."). Therefore, it is understood the active resistance device operates in the linear region. Fig. 2 shows current mirror

circuit 20 having first/second current paths 30,24,22/32,26 formed between first power source terminal U_{DD} and a second power source terminal (e.g. ground), wherein the current mirror circuit is operated in response to a voltage level of the second current path (e.g. via the voltage level between 32 and 26 being applied to the gate of 30); although a reference voltage output node is not specifically shown on the second current path (between 32 and 26) for providing a reference voltage (e.g. see page 9, line 22 "Transistor 26 abfallende Spannungsabfall U_{26}"), it would be obvious to one of ordinary skill in the art that the common node between 32 and 26 could be used to provide a reference voltage output node. Since active resistance device 22 is on the first current path, and operated in the linear region (as previously described), claims 6, and 13 are rendered obvious. Whatever circuitry (not shown) that provides enable voltage U_E to control active resistance device 22 is considered a voltage supply circuit, rendering claim 7 obvious. Since 22 is a single MOS transistor, and enable voltage U_E (e.g. 2 to 5 volts) would be higher than the drain to source voltage, claims 8-9 are rendered obvious. Also, it would have been obvious to one of ordinary skill in the art to replace active resistance device 22 with a plurality of series coupled N-channel MOS transistors that all receive the enable/control gate voltage, rendering claim 10 obvious. The single MOS transistor 22, shown in the figure, could be replaced by a functionally equivalent plurality of series coupled NMOS transistors to be used as the active resistance device depending on the overall size requirements of the elements (or circuit), and/or voltage levels required. For example, a plurality of series connected small MOS transistors can provide the same resistance (and voltage drop) as a single, large MOS transistor. To ensure the active resistance device's transistors operate in the linear region, the enable voltage applied to the gates would be higher than the drain to source voltages of the NMOS

transistors, and claim 11 is also rendered obvious. Current control unit 24,26, with MOS transistors 24/26 formed on the first/second current paths, respectively, controls the current flowing in those paths, rendering obvious claim 14. Since current mirror circuit 20 includes a pair of PMOS transistors 30/32 formed on the first/second current paths, respectively, claim 15 is also rendered obvious.

Claims 6-11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi, a reference found during the recent update search. Fig. 12 of Taguchi shows a reference voltage generating circuit that directly corresponds to the applicants' own Prior Art Fig. 2. Taguchi's reference comprises current mirror circuit 50,51 having first/second current paths 50,41,42/51,39 formed between first power source terminal 37 (receiving voltage VCC) and a second power source terminal (ground), wherein the current mirror circuit is operated in response to a voltage level (via the interconnections of the transistors) of the second current path; reference voltage output node 43, on the second current path, provides reference voltage Vref; and resistance device 42 is formed on the first current path. Although resistance device 42 is a passive device instead of an active resistance device, Taguchi discloses it as a load element (e.g. see column 7, lines 46-47), wherein Taguchi also discloses load elements can be a resistor or an insulated-gate field-effect transistor (e.g. see column 6, lines 20-23; and column 7, lines 19-23). Therefore, it would have been obvious to one of ordinary skill in the art to replace resistance device 42 with a FET (one known type of active resistance device) operated in a linear region, thus rendering claim 6 obvious. When operated in the linear (e.g. triode, resistive, nonsaturation, or ohmic) region, the active resistance FET device will function as a resistor with a resistance that varies with the FET's control gate voltage being higher than the drain to source voltage. The

FET would use less area than a resistor; help reduce power consumption; and allow the resistance to be changed (e.g. by adjustment of the gate voltage) to meet the desired requirement(s) of the overall circuit's use. Whatever circuitry that provides the control gate voltage/enable voltage to the active resistance device/FET can be deemed a voltage supply circuit, and claim 7 is rendered obvious. It would have been obvious to one of ordinary skill in the art that the active resistance FET device could be a single N-channel MOS transistor, or a plurality of series coupled N-channel MOS transistors that all receive the enable/control gate voltage, rendering claims 8 and 10 obvious. The single MOS transistor, or a functionally equivalent plurality of series coupled MOS transistors, can be used as the active resistance device depending on the overall size requirements of the elements (or circuit), and/or voltage levels required. For example, a plurality of series connected small MOS transistors can provide the same resistance (and voltage drop) as a single, large MOS transistor. To ensure the active resistance device's transistor(s) operates in the linear region, the enable voltage applied to the gate(s) would be higher than the drain to source voltage(s) of the N-channel MOS transistor(s), and claims 9 and 11 are rendered obvious. Since first power source terminal 37 receives externally applied voltage VCC, and the second power source terminal is connected to a ground voltage (not labeled but understood), claim 13 is also rendered obvious. The Fig. 12 circuit also comprises current control unit 41,39 for controlling current flowing in the first/ second current paths by employing MOS transistors 41,39 formed on the first/second current paths, respectively. These transistors render claim 14 obvious. Since current mirror circuit 50,51 includes a pair of PMOS transistors 50/51 formed on the first/second current paths respectively, claim 15 is also rendered obvious. Interpreting Fig. 12 in a slightly different manner, it shows a reference voltage

generating circuit comprising current mirror circuit 50,51 with first/second MOS transistors 50/51, wherein their sources receive externally applied voltage VCC, the gate of first MOS transistor 50 is connected to its drain, as well as to the gate of second MOS transistor 51; current control circuit 41,39 with third/fourth MOS transistors 41/39, wherein the drains of first/third MOS transistors 50/41 are connected together, the drain of fourth MOS transistor 39 is connected to the gate of third MOS transistor 41 and to the drain of second MOS transistor 51, and a source of fourth MOS transistor 39 is connected to ground. The node between the drains of the second/fourth MOS transistors 51/39 provides reference voltage Vref. However, the reference shows passive resistance circuit 42 coupled between the source of third MOS transistor 41/gate of fourth MOS transistor 39 and ground. As previously described above, Taguchi discloses the resistance circuit (e.g. load or resistor) can be replaced with a MOS transistor. Therefore, it would have been obvious to one of ordinary skill in the art to replace resistance circuit 42 with an active resistance circuit, such as an NMOS transistor. This would be the fifth MOS transistor within the reference voltage circuit, and would have its drain coupled to the source of third MOS transistor 41 and to the gate of fourth MOS transistor 39; its source connected to ground; and to ensure the fifth MOS transistor operates in the linear region to provide the proper resistance, its gate could receive a control voltage higher than the voltage between the transistor's drain and source. Therefore, claim 16 is rendered obvious.

No claim is allowable as presently written.

Claims 2 and 4 have been cancelled.

Allowable Subject Matter

However, claim 12 is only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is no strong motivation to modify or combine any prior art reference(s) to ensure the voltage supply circuit includes the PMOS, and plurality of NMOS, transistors as recited within claim 12.

Also, claims 17-18 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is no strong motivation to modify or combine any prior art reference(s) to ensure the voltage supply circuit includes the PMOS and set of NMOS transistors as recited within claim 17, upon which claim 18 depends.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to the claimed inventions. Abraham et al. shows/discloses a linear active resistor comprising a plurality of series coupled transistors (e.g. see 23 and 21 in Fig. 2), and discloses "on-die resistors can be created using transistors operated in the so-called "linear region"" on column 1, lines 43-44. Park shows similar reference voltage generating circuits in Figs. 4 and 5, wherein Fig. 4 shows transistor M47, and Fig. 5 shows resistor R, thus implying that they are functionally equivalent. Park also discloses transistor M47 operates in the linear region (e.g. see column 3, lines 41-42). Fig. 3 of Shin et al., shows a plurality of MOS transistors NM5-NM7 with their gates commonly connected to enable voltage VCC. Although this reference does not clearly indicate the transistors operate in a linear current-voltage region, Shin discloses transistors NM5-

NM7 are used as an MOS resistor with a resistance that varies with VCC (e.g. see column 5, lines 5-12). Also, the reference discloses that only one of the three transistors could be used (e.g. see column 4, lines 46-50, and column 7, lines 22-26). Therefore, these circuits, as well as the (implicitly or explicitly) disclosed teachings, should be carefully reviewed and considered with respect to the claimed limitations within the present application.

Response to Arguments

The applicants' argument/comments filed Dec 6, 2004, with respect to the connection of Q13's source to its gate, have been fully considered but are not persuasive. The amendment's page 10 cites "Fig. 3 also shows the source of the transistor Q13 connected to its gate.", and page 11 cites "Figs. 3 and 5, both of which show a gate of a PMOS transistor (e.g., transistors Q13 and Q31) connected to its source." Although the figures do show the source connected to the back gate of the transistor, the back gate is not the same as the transistor's (control) gate. Therefore, the source and gate are clearly not connected together as the disclosure, and claim 17, describes. Also, it should be noted that if the applicants insist the gate and source are actually connected together, then Evcc is connected to the gates of all the PMOS transistors shown (i.e. Q8, Q9, and Q13 in Fig. 3; and Q17, Q18, and Q31 in Fig. 5). In such a configuration, the PMOS transistors would always be off, and the applicants' circuit will not operate. Therefore, clarification is requested with respect to what the applicants actually consider the gate of transistor Q13 (or Q31).

The applicants also argue that the reference of Viehmann does not disclose a reference voltage output node (located on the second current path). Although page 13 of the amendment indicates there is no reference voltage node for providing a reference voltage along either current

path, that is only true if one insists that a node must be clearly shown and/or identified as an output node providing a reference voltage. For example, one of ordinary skill in the art would understand the common node between transistors 30 and 24 in the first current path is one type of output node. Although it is not labeled, it does provide a reference voltage to the gate of transistor 28. However, since the Viehmann reference does not specifically show a reference voltage being provided at an output node on the second current path, the previous Office Action's claim rejections under 35 U.S.C. 102(b) have been withdrawn. New, obvious type rejections are now described above with respect to the Viehmann reference.

Since the applicants argue that their own Prior Art Fig. 2 does not provide sufficient teachings or suggestions to make the obviousness type rejections described in the previous Office Action, an update search was performed. A reference, showing a circuit that directly corresponds to the applicants' Fig. 2, was found that teaches a resistor can be replaced by a MOS transistor. Therefore, the claims are still rejected, but with a reference that provides suitable support for the reasoning used within the rejections.

Therefore, the claim rejections are deemed proper with respect to what one of ordinary skill in the art would understand.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

15 March 2005

Terry D. Cunningham
Primary Examiner